INTEGRATED CIRCUIT CAPACITORS HAVING DOPED HSG ELECTRODES

Cross-Reference to Related Application

This application is a divisional of U.S. Application Serial No. 09/735,244, filed December 12, 2000, which is a continuation of U.S. Application Serial No. 09/036,356, filed March 6, 1998, now U.S. Patent No. 6,218,260, the disclosures of which are hereby incorporated herein by reference.

Field of the Invention

The present invention relates to methods of forming integrated circuits and circuits formed thereby, and more particularly to methods of forming integrated circuit capacitors and capacitors formed thereby.

Background of the Invention

The demand for higher capacity semiconductor memory devices has resulted in improved techniques to form memory devices and structures therein at higher levels of integration. However, because higher levels of integration typically require memory devices having smaller unit cell size, the area occupied by a cell capacitor in a memory device, such as a DRAM device, may have to be reduced significantly. As will be understood by those skilled in the art, this reduction in cell capacitor area can degrade memory cell performance at low voltages and adversely impact soft-error rate (SER) caused by α-particle radiation.

Conventional methods of increasing cell capacitor area include forming cell capacitor electrodes (e.g., storage electrodes) with hemispherical grain (HSG) silicon surface layers. For example, a conventional method of forming HSG silicon surface layers on cell capacitor electrodes is disclosed in U.S. Patent No. 5,407,534 to Thakur. However, while capacitors having HSG surface layers therein (hereinafter "HSG capacitors") have manifested enhanced capacitance in high density integrated circuits, HSG capacitors may lack stability and may incur performance degradation over the lifetime of an integrated circuit memory device. Studies have shown that the capacitance of a conventional HSG capacitor can vary greatly with respect to the